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	Application No.	Applicant(s)	411
Nada - PAH	10/719,818	HORETH, STEFAN	
Notice of Allowability	Examiner	Art Unit	
	James Cho	2819	
The MAILING DATE of this communication appeal claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this applied or other appropriate communication IGHTS. This application is subject to	plication. If not include will be mailed in due	ed course. THIS
1. X This communication is responsive to the application file 11	<u>-21-2003</u> .		
2. The allowed claim(s) is/are <u>1-10</u> .			
3. \boxtimes The drawings filed on <u>21 November 2003</u> are accepted by	the Examiner.		
4. Acknowledgment is made of a claim for foreign priority una a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority do International Bureau (PCT Rule 17.2(a)). * Certified copies not received: Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE. 5. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give 6. CORRECTED DRAWINGS (as "replacement sheets") must	e been received. e been received in Application No cuments have been received in this of this communication to file a reply IENT of this application. itted. Note the attached EXAMINER es reason(s) why the oath or declara	national stage applicate complying with the reconstruction.	quirements
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 (a) ☐ including changes required by the Notice of Draftspers 1) ☐ hereto or 2) ☐ to Paper No./Mail Date 		946) allached	
(b) ☐ including changes required by the attached Examiner' Paper No./Mail Date		office action of	
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t			back) of
 DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT 			Note the
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date 11-21-03 4. ☐ Examiner's Comment Regarding Requirement for Deposit	5. ☐ Notice of Informal P 6. ☑ Interview Summary Paper No./Mail Dat 7. ☑ Examiner's Amendn 8. ☑ Examiner's Stateme	(PTO-413), le <u>6-9-05</u> . nent/Comment	
of Biological Material	9.		

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Peter Corless on June 9, 2005.

The application has been amended as follows:

IN THE SPECIFICATION:

The abstract has been replaced with following:

- In order when designing a digital circuit to be able to determine the minimum or maximum switching activity for estimating the power consumption it is determined according to the invention on the basis of a model of the digital circuit whether there is a disproving operational case, in which the switching activity is less than an estimated value (k) for the minimum switching activity or greater than an estimated value (k) for the maximum switching activity. If the existence of an appropriate disproving operational case (P(k)) can be found, when determining the maximum switching activity the estimated value (k) is increased by one step size and when determining the minimum switching activity the estimated value (k) reduces. After a decrease or increase of the estimated value (k) the process is repeated and in this way the actual value for the maximum or minimum switching activity of the digital circuit is determined iteratively.

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After an appropriate interruption condition the currently used estimated value (k) is employed as the measure for the minimum or maximum switching activity. Based on the minimum or maximum switching activity on the one hand the minimum or maximum power consumption of the digital circuit can be determined or on the other hand further diagnostic functions can be carried out.--

On the top of page 10, the wording, --Brief Description of Drawings-- has been inserted before the first line.

Allowable Subject Matter

Claims 1-10 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: Although Roethig et al. (US PAT No. 6,625,781) discloses multi-level power macromodeling, one of ordinary skill in the art would not have been motivated to modify the teaching of Roethig et al. to further includes, among other things, the specific of determining a minimum or maximum switching activity by performing a method, with which method for determining the minimum switching activity a check is performed as to whether there is at least one disproving operational case of the digital circuit, in which the switching activity is less than an estimated value, and the check is repeated if there is a disproving operational case with an estimated value reduced by one step size and if there is no disproving operational case with an estimated value increased by one step size as set forth in the claims.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dey et al. (US PAT No. 6,105,139) discloses controller-based power management for low-power sequential circuits.

Sako (US PAT No. 6,185,719) discloses a method of designing pass-transistor logic circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

لرames H. Cho Primary Examiner Art Unit 2819

June 9, 2005